

REMARKS

Claims 1-7 were examined and reported in the Office Action. Claims 1-3 are rejected. Claims 4-7 are amended. New claims 8-14 are added. Claims 1-14 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. § 102(e)

It is asserted in the Office Action that claims 1-3 are rejected under 35 U.S.C. § 102(e), as being anticipated by Pub. No. U.S. 2003/0030473 issued to Lee ("Lee"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2131, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990))."

Applicant's amended claim 1 contains the limitations of "[a] delay locked loop (DLL) block to generate a delay locked clock signal by delaying an external clock signal in a semiconductor device, comprising: a clock buffer to receive the external clock signal and an inverted signal of the external clock signal to generate a plurality of internal clock signals; a clock divider to receive one of the internal clock signals and a control signal based on a column address strobe (CAS) signal to generate a divided signal having a predetermined pulse width adjusted by the control signal; and a DLL circuit to receive the plurality of internal clock signals and the divided signal to generate the delay locked clock signal."

In Applicant's claimed invention the clock divider generates a divided signal where each portion has a different pulse width according to the column address strobe (CAS) latency. Since the CAS latency changes according to operational frequency, the pulse width of the divided signal is adjusted according to the operational frequency. Therefore, the delay locked loop (DLL) (including the divided signal) can be operated both at a high operational frequency and a low operational frequency.

Lee discloses a ring-resister controlled DLL with a fine delay line and a direct skew sensing detector that is applicable to circuitry for compensating skew between external and internal clocks. Lee, however, does not teach, disclose or suggest adjusting pulse width of a divided signal. That is, Lee does not teach, disclose or suggest "a clock divider to receive one of the internal clock signals and a control signal based on a column address strobe (CAS) signal to generate a divided signal having a predetermined pulse width adjusted by the control signal; and a DLL circuit to receive the plurality of internal clock signals and the divided signal to generate the delay locked clock signal." Note that, according to Lee, since the pulse width of a divided signal is fixed, Lee's DLL is suitable for a fixed operational frequency range.

Therefore, since Lee does not disclose, teach or suggest all of Applicant's amended claim 1 and new claim 8 respective limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(e) has not been adequately set forth relative to Lee. Thus, Applicant's amended claim 1 and new claim 8 are not anticipated by Lee. Additionally, the claims that directly or indirectly depend from claims 1 and 8, namely claims 2-3, and 9-14, respectively, are also not anticipated by Lee for the same reasons.

Accordingly, withdrawal of the 35 U.S.C. § 102(e) rejection for claims 1-3 is respectfully requested.

II. Allowable Subject Matter

Applicant notes with appreciation the Examiner's assertion that claims 4-7 are objected to as being dependent upon a rejected base claim, but would be allowable if

rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant respectfully asserts that claims 1-14, as it now stands, are allowable for the reasons given above.

CONCLUSION

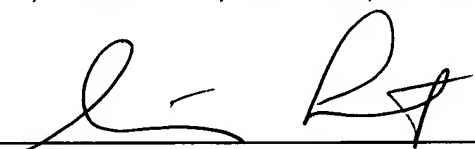
In view of the foregoing, it is submitted that claims 1-14 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

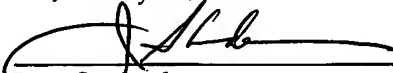
Dated: January 26, 2005

By: 
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on January 26, 2005.


Jean Svoboda